AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An array-type processor comprising:

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, said multiplicity of processor elements arranged in rows and columns on the array-type processor; and

a plurality of state control units which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas;

said state control units are connected to the plurality of element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and

said state control units temporarily halt operations of said element areas that correspond to a prescribed number of said operating states that are set to one said context during said operating cycles in which said operating states do not occur; and

said state control unit individually and temporarily halts said plurality of element areas.

2. (currently amended): An array-type processor comprising:

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, said multiplicity of processor elements arranged in rows and columns on the array-type processor; and

state control units which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a plurality of element areas;

each of the plurality of element areas is connected to a respective state control unit of an equal number of the element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts; and

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur; and

said plurality of state control units individually and temporarily halt said plurality of element areas.

3. (currently amended): An array-type processor comprising:

a multiplicity of processor elements, which individually execute data processing in accordance with instruction codes in which data are individually set, said multiplicity of processor elements arranged in rows and columns on the array-type processor; and

state control units which change a configuration of the multiplicity of processor elements and cause successive transitions of operating states of the multiplicity of processor elements for each operating cycle by contexts that are composed of said instruction codes; wherein:

said multiplicity of processor elements are divided into a number (a×b) of element areas;

each of a number (a) of said state control units is connected to a respective group of (b) element areas of these (a×b) element areas;

a prescribed number of said operating states that occur in different said operating cycles are set to at least a portion of said contexts;

said state control units temporarily halt operations of said element areas to which said state control units are connected, the operations of the element areas corresponding to a prescribed number of said operating states that are set to one said context, during said operating cycles in which said operating states do not occur; and

said plurality of state control units individually and temporarily halt said plurality of element areas.

4. (original): An array-type processor according to claim 1, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

5. (original): An array-type processor according to claim 2, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

6. (original): An array-type processor according to claim 3, wherein said state control units cause an operation of a portion of a plurality of processor elements of said element areas that said state control units have temporarily halted.

7. (original): An array-type processor according to claim 1, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

8. (original): An array-type processor according to claim 2, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

9. (original): An array-type processor according to claim 3, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

10. (original): An array-type processor according to claim 4, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

11. (original): An array-type processor according to claim 5, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

12. (original): An array-type processor according to claim 6, wherein:

a shared resource is provided that is shared by said plurality of element areas; and

said state control units switch paths to said shared resource from said plurality of element areas.

13. (new): An array-type processor according to claim 1, wherein the plurality of processing elements are connected by a datapath on a common substrate.

14. (new): An array-type processor according to claim 2, wherein the plurality of processing elements are connected by a datapath on a common substrate.

15. (new): An array-type processor according to claim 3, wherein the plurality of processing elements are connected by a datapath on a common substrate.